Abstract of the Disclosure:

A comparison method compares the address of a memory cell with a known address of a faulty memory cell in a semiconductor memory module. The module is subdivided into banks and has an address structure in which each address is associated with a bank that is organized in rows and columns and is defined by a row address, a column address and a bank address. Not only the row address is determined, but also the column address and the bank address when a memory access occurs. A bank is activated with a bank selection signal, and the access to a valid address of a faulty memory cell is indicated by an enable register.

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